

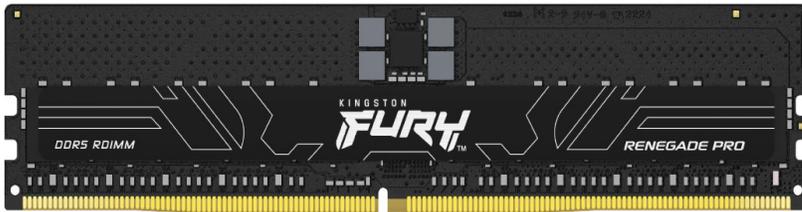


Memory Module Specifications

KF556R36RB-32

32GB 1Rx4 4G x 80-Bit

PC5-5600 CL36 Registered EC8 288-Pin DIMM



DEFAULT SPECIFICATIONS

CL(IDD)	40 cycles
Row Cycle Time (tRCmin)	48ns(min.)
Refresh to Active/Refresh Command Time (tRFCmin)	295ns(min.)
Row Active Time (tRASmin)	32ns(min.)
Row Precharge Time (tRPmin)	16ns(min.)
UL Rating	94 V - 0
Operating Temperature	0° C to +95° C
Storage Temperature	-55° C to +100° C

DESCRIPTION

Kingston FURY KF556R36RB-32 is a 4G x 80-bit (32GB) DDR5-5600 CL36 SDRAM (Synchronous DRAM) 1Rx4, ECC memory module, based on twenty 4G x 4-bit FBGA components per module. The module supports Intel® Extreme Memory Profiles (Intel® XMP) 3.0. Each module has been tested to run at DDR5-5600 at a low latency timing of 36-38-38 at 1.25V. The SPDs are programmed to JEDEC standard latency DDR5-4800 timing of 40-39-39 at 1.1V. Each 288-pin DIMM uses gold contact fingers. The JEDEC standard electrical and mechanical specifications are as follows:

FACTORY TIMING PARAMETERS

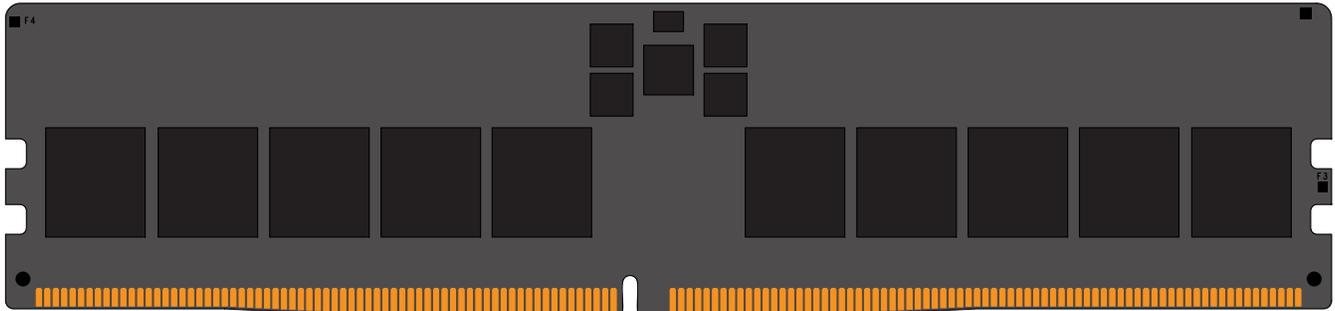
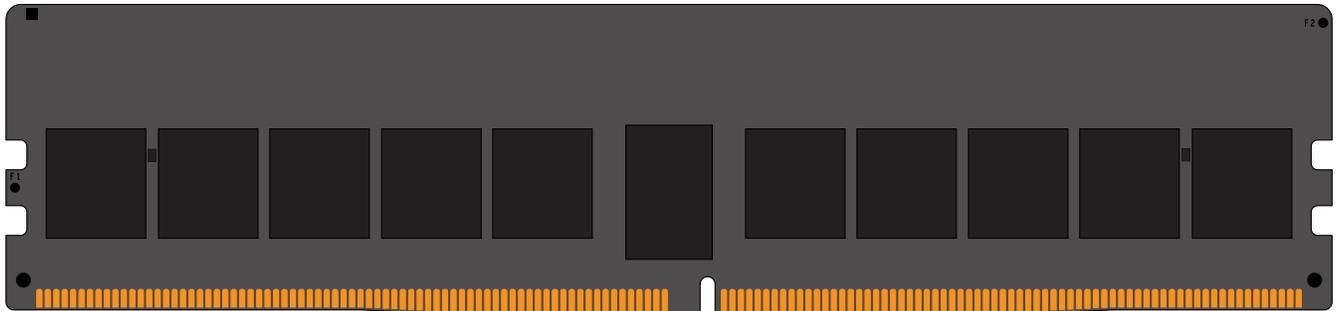
- Default (JEDEC): DDR5-4800 CL40-39-39 @1.1V
- XMP Profile #1: DDR5-5600 CL36-38-38 @1.25V
- XMP Profile #2: DDR5-5200 CL36-40-40 @1.25V
- XMP Profile #3: DDR5-4800 CL36-38-38 @1.1V

DEFAULT FEATURES

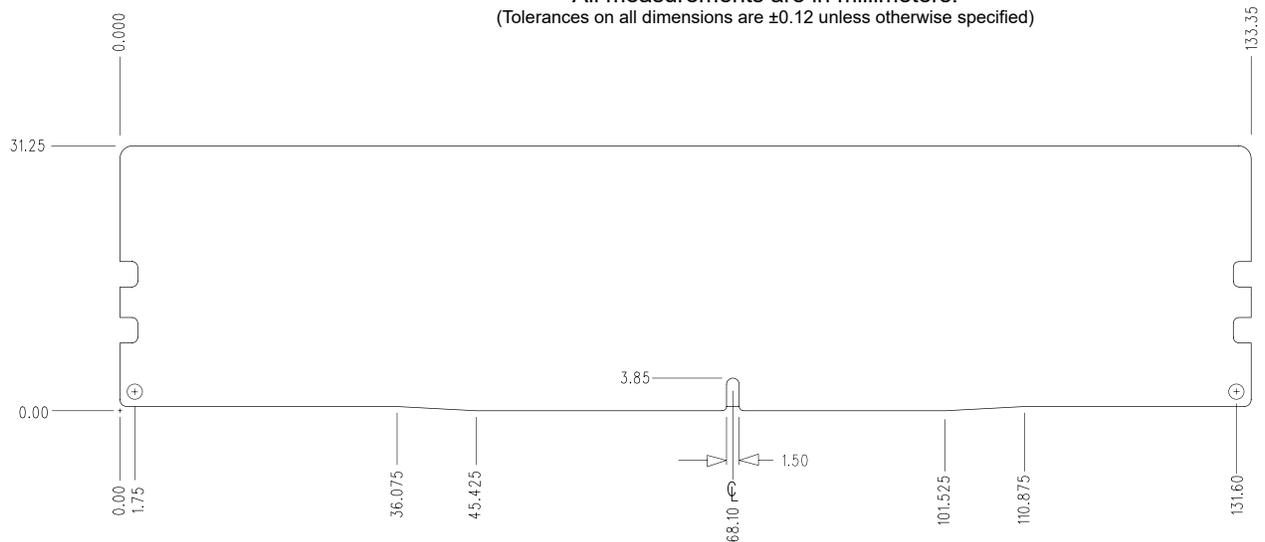
- Power Supply: VDD = 1.1V Typical
- VDDQ = 1.1V Typical
- VPP = 1.8V Typical
- VDDSPD = 1.8V to 2.0V
- On-Die ECC
- x80 ECC (x40, 2 independent I/O sub channels)
- 32 internal banks
- Hard/Soft Post Package Repair
- Sideband access with I3C/I2C
- PCB: Height 1.23" (31.25mm)
- RoHS Compliant and Halogen-Free

Continued >>

MODULE DIMENSIONS



All measurements are in millimeters.
(Tolerances on all dimensions are ± 0.12 unless otherwise specified)



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All Kingston products are tested to meet our published specifications. Some motherboards or system configurations may not operate at the published Kingston FURY memory speeds and timing settings. Kingston does not recommend that any user attempt to run their computers faster than the published speed. Overclocking or modifying your system timing may result in damage to computer components.

Revision No.	History	Release Date	Remark	Editor	Approved
A	Initial Release	3/16/2023		David Y.	Tuan H.
B	Change measurements (pg2)	4/25/2023		David Y.	Tuan H.

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